IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Currently Amended) A method for reducing leakage current in a read only memory array having a plurality of transistors, comprising the step of:

applying a biased gate voltage, relative to a source voltage, to the gate of ~~at least one~~ each of said plurality of transistors, said biased gate voltage to be applied at least during a precharge phase.

2. (Original) The method of claim 1, wherein said plurality of transistors are n-channel transistors and wherein said biased voltage is a negative bias voltage relative to said source voltage.

3. (Original) The method of claim 2, further comprising the step of applying a negative bias voltage, with respect to the source, to a p-well of said at least one of said plurality of transistors.

4. (Original) The method of claim 1, wherein said plurality of transistors are p-channel transistors and wherein said biased voltage is a positive bias voltage relative to said source voltage.

5. (Original) The method of claim 4, further comprising the step of applying a positive bias voltage, with respect to the source voltage, to an n-well of said at least one of said plurality of transistors.

6. (Currently Amended) The method of claim 1, wherein said biased gate voltage is applied only during a precharge phase of a read cycle.

7. (Original) The method of claim 1, wherein said biased gate voltage is applied during a standby phase.

8. (Currently Amended) A method for reducing leakage current in ~~an~~ a read only memory array having a plurality of transistors, comprising the step of:

applying a first potential to a drain terminal of each of said plurality of transistors to be programmed;

applying a second potential to a gate terminal of at least one of said plurality of transistors during a precharge phase;

applying a third potential to a source terminal of at least one of said plurality of transistors; and

applying a fourth potential to a well contact of at least one of said plurality of transistors, wherein the third potential is of substantially different value than the second potential.

9. (Original) The method of claim 8, wherein the read only memory array is an n-channel memory array.

10. (Original) The method of claim 8, wherein the second potential is equal to the fourth potential.

11. (Original) The method of claim 9, wherein the third potential is positive, and the second and fourth potential are 0 volts.

12. (Original) The method of claim 8, wherein the third potential is between but not equal to the second and first potentials.

13. (Original) The method of claim 9, wherein the third potential is approximately 0.1 to 0.3 volts.

14. (Original) The method of claim 8, wherein the read only memory array is a p-channel memory array.

15. (Original) The method of claim 14, wherein the first potential is approximately zero volts, and the second and fourth potential are a positive voltage.

16. (Original) The method of claim 14, wherein the third potential is approximately 0.1 to 0.3 volts lower than said second potential.

17. (Currently Amended) A read only memory array, comprising:

a plurality of transistors each having a gate terminal adapted to be substantially simultaneously coupled to a biased gate voltage, relative to a source voltage, said biased gate voltage to be applied at least during a precharge phase.

18. (Original) The read only memory array of claim 17, wherein said plurality of transistors are n-channel transistors and wherein said biased voltage is a negative bias voltage relative to said source voltage.

19. (Original) The read only memory array of claim 18, wherein said read only memory array is further configured to apply a negative bias voltage, with respect to the source, to a p-well of said at least one of said plurality of transistors.

20. (Original) The read only memory array of claim 17, wherein said plurality of transistors are p-channel transistors and wherein said biased voltage is a positive bias voltage relative to said source voltage.

21. (Original) The read only memory array of claim 20, wherein said read only memory array is further configured to apply a positive bias voltage, with respect to the source voltage, to an n-well of said at least one of said plurality of transistors.

22. (Currently Amended) The read only memory array of claim 17, wherein said biased gate voltage is applied only during a precharge phase of a read cycle.

23. (Original) The read only memory array of claim 17, wherein said biased gate voltage is applied during a standby phase.

24. (Original) A read only memory array, comprising:

a plurality of transistors, wherein each of said plurality of transistors to be programmed has a drain terminal adapted to be coupled to a first potential and wherein at least one of said transistors further comprises:

a gate terminal adapted to be coupled to a second potential during a precharge phase;

a source terminal adapted to be coupled to a third potential; and

a well contact adapted to be coupled to a fourth potential, wherein the third potential is of substantially different value than the second potential.

25. (Original) The read only memory array of claim 24, wherein the read only memory array is an n-channel memory array; the second potential is equal to the fourth potential; the first potential is positive, and the second and fourth potential are 0 volts and the third potential is between but not equal to the second and first potentials.

26. (Original) The read only memory array of claim 24, wherein the read only memory array is a p-channel memory array; the first potential is approximately zero volts, and the second and fourth potential are a positive voltage, and the third potential is between but not equal to the second and first potentials. .

27. (Currently Amended) An integrated circuit, comprising:

a read only memory array, comprising a plurality of transistors each having a gate terminal adapted to be substantially simultaneously coupled to a biased gate voltage, relative to a source voltage, said biased gate voltage to be applied at least during a precharge phase.

28. (Original) The integrated circuit of claim 27, wherein said plurality of transistors are n-channel transistors and wherein said biased voltage is a negative bias voltage relative to said source voltage.

29. (Original) The integrated circuit of claim 28, wherein said read only memory array is further configured to apply a negative bias voltage, with respect to the source, to a p-well of said at least one of said plurality of transistors.

30. (Original) The integrated circuit of claim 27, wherein said plurality of transistors are p-channel transistors and wherein said biased voltage is a positive bias voltage relative to said source voltage.

31. (Original) The integrated circuit of claim 30, wherein said read only memory array is further configured to apply a positive bias voltage, with respect to the source voltage, to an n-well of said at least one of said plurality of transistors.

32. (Currently Amended) The integrated circuit of claim 27, wherein said biased gate voltage is applied only during a precharge phase of a read cycle.

33. (Original) The integrated circuit of claim 27, wherein said biased gate voltage is applied during a standby phase.